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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/903,760	07/13/2001	Yoshifumi Takata	50090-318	2858

7590 10/16/2002

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Washington, DC 20005-3096

EXAMINER

MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
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2827

DATE MAILED: 10/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/903,760

Applicant(s)

TAKATA ET AL.

Examiner

James Mitchell

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9,11 and 12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9,11 and 12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7.
- 5) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano (U.S 6,022,804) in combination with Gwon (000266749B1) and Tottori.

Yano (Fig 1(a)-2) discloses a method of forming a semiconductor device comprising the steps of: forming a silicon oxide containing phosphor ("BPSG") first interlayer (21) on a semiconductor substrate (1), forming a plurality of openings (Fig 1e) in said first interlayer insulating film, forming a conductor (51) on said first interlayer insulating film so as to fill said openings and removing said conductor film from said surface of said first interlayer insulating film through chemical etching (Column 12, Lines

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60-65) and forming conductor plugs ("contacts") from said conductor film, forming a second interlayer insulating film (22) on said first interlayer insulating film, forming a wiring pattern (41B) on said second insulating film, forming a third interlayer insulating film (23) on said second insulating film so as to cover said wiring pattern and forming a plurality of openings so as to penetrate said second and third interlayer insulating film respectively to said conductor plug, and forming a plurality of interconnect conductors (43B) in said openings so as to be electrically connected to each of said conductor plugs.

Yano does not appear to disclose leveling the surface of the first interlayer insulating film from which the conductor has been removed until the surface of the first interlayer insulating film becomes flush with the surface of the conductor plug by CMP, or that the contacts are comprised of a polycrystalline silicon.

However Sato utilizes CMP after an etch step (shown in Fig 1; Column 3, Lines 1-15) comprising: removal of a conductor from insulating film through a chemical etch ("RIE") to form a plug ("metal contact") from said conductor filled in an opening and then leveling (Column 4, Lines 6-12) the surface of said insulating film from which the conductor film has been removed until the surface of the insulating film and plugs are flush by CMP.

It would have been obvious to one of ordinary skill in the art to incorporate a CMP step after an etch step to the interconnect structure of Yano, in order to eliminate inferior coverage as taught by Sato (Column 2, Lines 45-46, 59-64).

Tottori utilizes a polycrystalline silicon film to form a plug (Fig 1, Item 7; Abstract).

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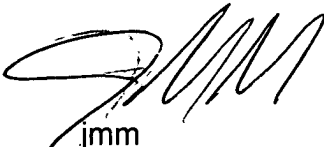
It would have been obvious to one of ordinary skill in the art to incorporate a polycrystalline silicon to the interconnect structure of Yano and Sato in order to form a conductive contact providing increased reliability as taught by Tottori (Column 4, Lines 38-40).

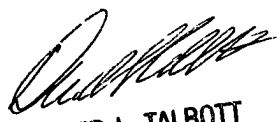
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


jmm
October 7, 2002


DAVID L. TALBOTT
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800